Monthly Report for

12-Bit High Dynamic Range ADC

Reporting Period: 15 March 1999 to 15 April 1999

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1.0 Technical Progress

During this reporting period, the top level mask revisions for the GaAs HBT ADC chip were completed, and the detailed design of the ADC MCM was initiated.

Top level mask revisions (i.e., resistor and interconnect metal changes only) were implemented to address five design issues identified as a result of the Phase 1 Breadboard evaluation. A brief description of each problem and its corresponding corrective action is given below:

- Large (MSB) code errors at high sample rates: this was addressed by increasing both the allocated regeneration time and the track-mode gain of the comparator gain to reduce its metastable probability (false code generation).
- Large (MSB) code errors at low sample rates: this was addresed by changing the timing signal to the coarse data latches (to avoid potential hold time violation), and by adding R-C damping to the corresponding clock buffers (to avoid parasitic oscillation or ringing problems).
- Poor large-signal distortion (SFDR): this was addressed by re-wiring the exisitng 2-pole lowpass filter in the ADC front-end to form a single-pole filter. A minor degradation in SNR and gain flatness is expected (this compromise will be eliminated in the final all-level design iteration).
- LSB code errors at low sample rates: this was addressed by increased clock damping (to avoid oscillation/ringing), revised clock bus routing (to minimize crosstalk), and increased time constant in the output flip-flops (to minimize a potential master/slave race condition).
- Temperature sensor oscillations: this was addressed by an output phase inversion (to eliminate the relaxation oscillation mode), and by a revised hysteresis design in the temperature comparator (to eliminate metastability problems).

The basic philosophy behind these top level changes was to implement them as an experiment designed to validate/correlate causes and effects. The results of these experiments will be used to implement a final, optimized all-level design. The top-level changes were

therefore strategically distributed across 4 variations of the baseline chip. A fifth (no change) version was included as a control.

Additional breadboard characterization was also performed to identify any additional potential design issues. None of these test results showed any additional chip anamolies. Figures 1 through 3 summarize the additional characterization data.

The detailed design ADC MCM was initiated. Some early problems were encountered with locating vendors to supply die versions of the COTS calibration components. Persistent searching has provided sources for most of the calibration components. The only remaining uncertainty is for the Actel FPGA – however, we expect this to be resolved by the next reporting period.

2. Plans for Next Reporting Period

During the next reporting period, the ADC MCM design will continue, and the detailed design of the all-level ADC IC iteration will be initiated.

3. Financial Status

Table 1 shows the forecasted versus actual expenditures for the Phase 2 program. At month-end March, 1999 the cumulative actuals were $56.9K versus a forecast of 65.0K. Figure 4 shows the development schedule for the Phase 2 activities.

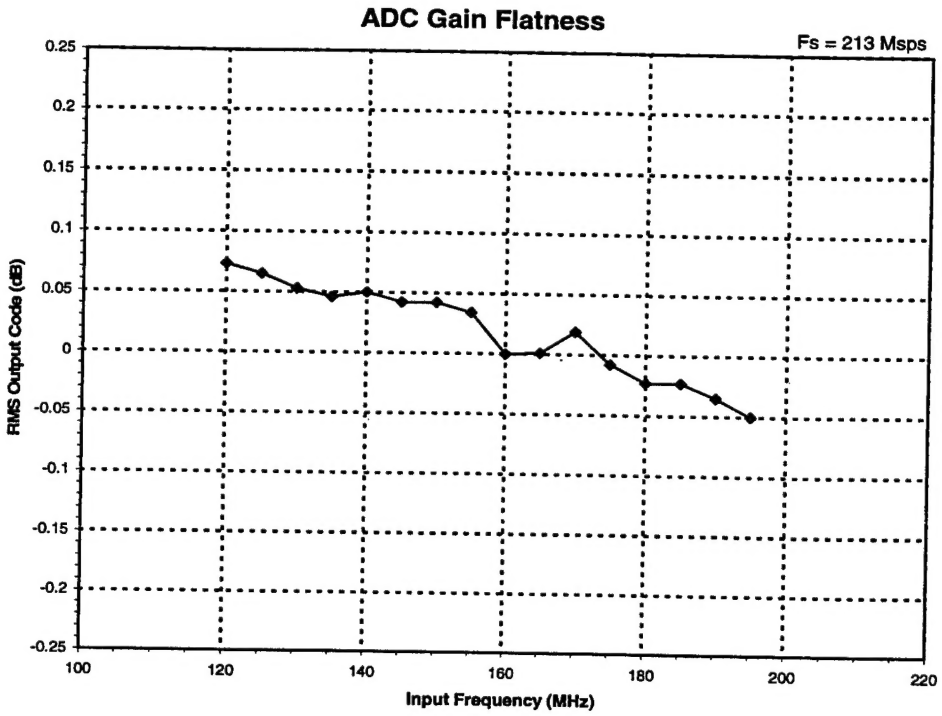

Figure 1. ADC Gain Flatness: ADC RMS Output Code (relative to midband) versus Input Frequency (Fin = 120 MHz to 190 MHz, Fs = 213 Msps).

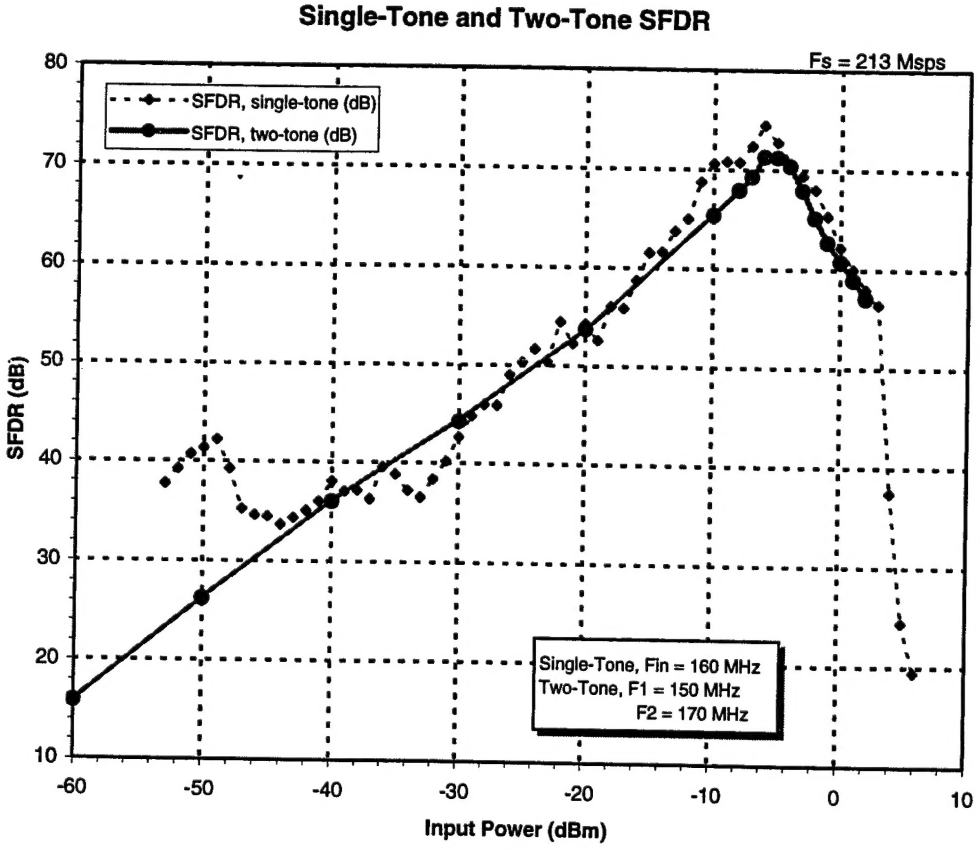

Figure 2. ADC Single-Tone versus Two-Tone SFDR Performance

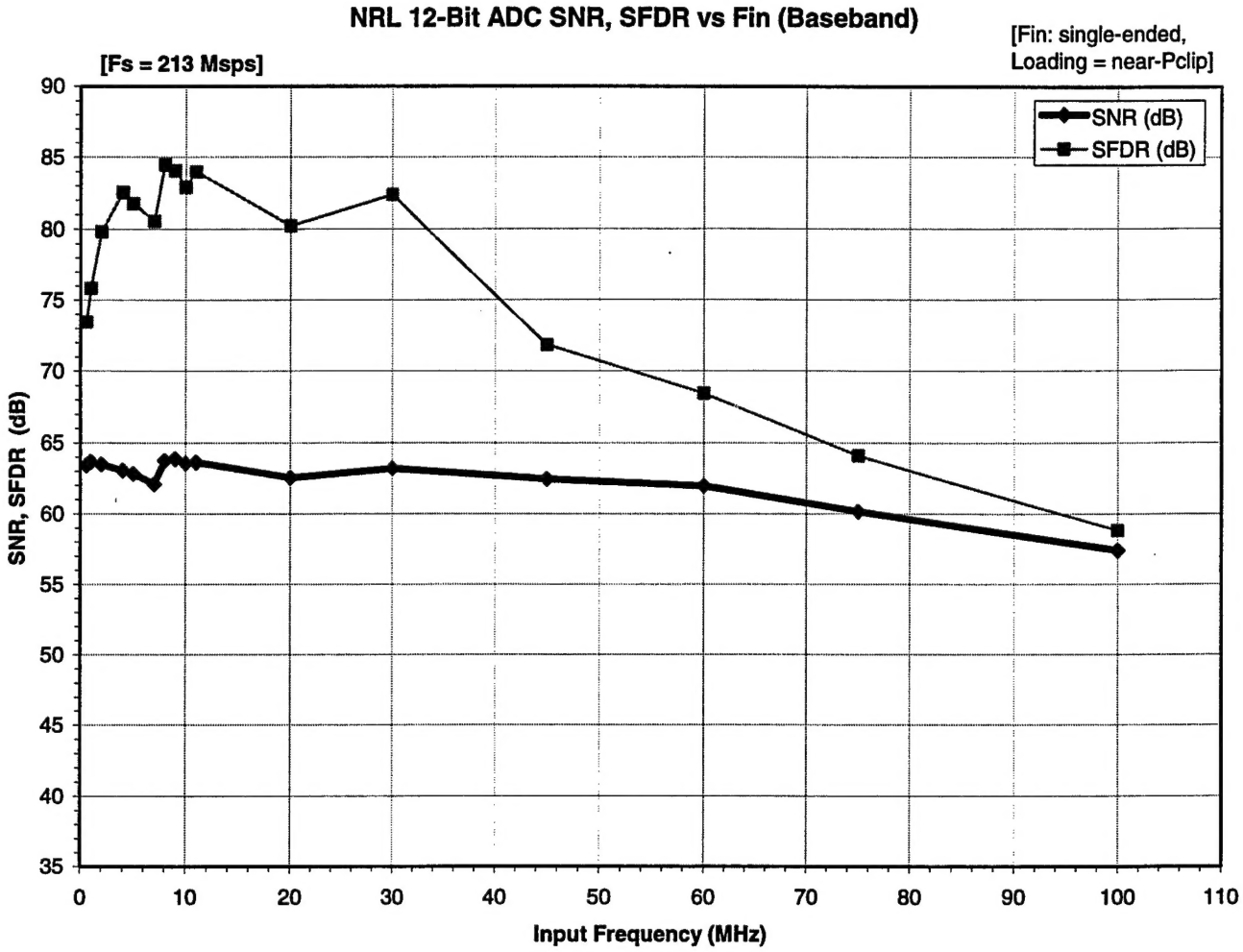

Figure 3. ADC Baseband Performance: SNR and SFDR versus Fin for Single-Ended Analog Input (no input transformer).

Table 1. Phase 2 Expenditures Forecast

Month	Monthly Total ($K)	Cumulative Total ($K)	Cumulative Actuals ($K)	Delta (Forecast - Actuals)
Mar-99	65.0	65.0	56.9	8.1
Apr-99	109.4	174.4		
May-99	100.8	275.2		
Jun-99	107.5	382.7		
Jul-99	45.9	428.6		
Aug-99	32.1	460.7		
Sep-99	79.6	540.3		
Oct-99	74.6	614.9		
Nov-99	27.0	641.9		
Dec-99	15.1	657.0		

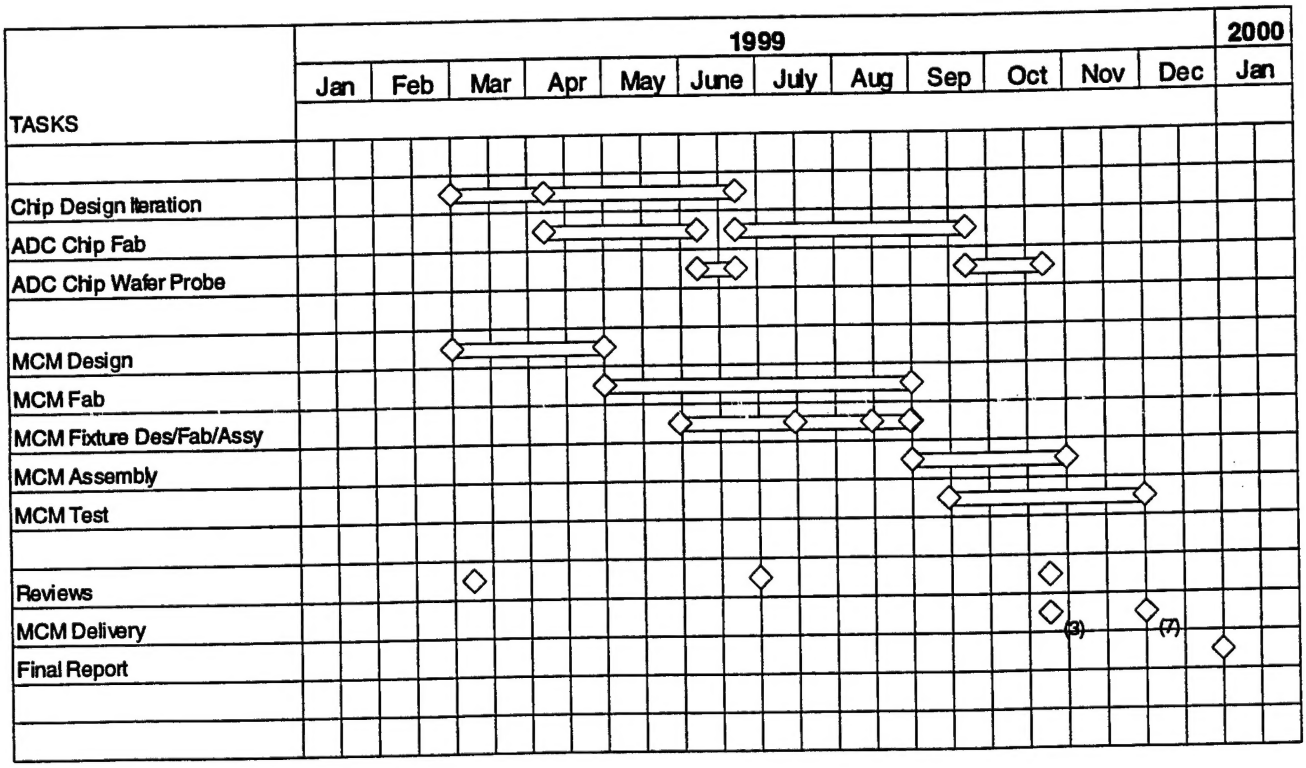

Figure 4. Development Schedule for Phase 2 Activities.